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(54) MICRO INTERCONNECTION CIRCUIT DEVICE AT ORIGINAL POSITION AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method for interconnection at the original position whereby nano-wires are grown and formed at the original position on each of circuit boards to create a structure of the interconnected nano-wires on each circuit board.
SOLUTION: Two parallel circuit boards 10, 10' are disposed with a fixed space (g), and catalyst nucleus forming layer 26 for selectively growing the nano-wires 14 are provided on pad surfaces with contact pads 12a, 12a' facing those 12b, 12b'. The nano-wires 14 grow to the mutually opposite sides to attain the interconnection at the original position.

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CLAIMS

[Claim(s)]

[Claim 1] They are the 1st circuit base, the 2nd circuit base, and a method of manufacturing two or more circuit apparatus which have been arranged among them, which contain an parallel nano wire substantially and which interconnected at least. Said 1st circuit base and the 2nd circuit base are aligned at least by relation parallel to the real target which vacated spacing. The step which demarcates a clearance among them, and the step which deposits a catalyst nucleation layer on said 1st circuit base at least, How to contain at least the step which carries out growth formation of said two or more nano wires from said catalyst nucleation layer on said 1st circuit base, and the step which offers the circuit apparatus which connected said nano wire which carried out growth formation at said 2nd circuit base, and interconnected.

[Claim 2] Said nano wire is an approach according to claim 1 characterized by carrying out growth formation horizontally to said 1st circuit base at least.

[Claim 3] Said 1st circuit base and the 2nd circuit base at least are an approach according to claim 2 characterized by including the semiconductor wafer which has the slot demarcated by them.
[Claim 4] The approach according to claim 3 characterized by including further the step which combines one or more electronic instruments with said circuit apparatus which interconnected.
[Claim 5] In order to demarcate the 1st contact pad and the 2nd contact pad at least with at least two circuit bases Since the contact pad prepared in each at least one of said the at least two circuit bases and said two circuit bases are interconnected Were prepared between said 1st contact pad and said 2nd contact pad. It aligns in the direction are the approach of manufacturing two or more circuit apparatus which contain an parallel nano wire substantially and which interconnected, and parallel to the real target which vacated spacing for said two circuit bases. The step which is a step which demarcates among them the clearance which has predetermined magnitude, meets and aligns said 1st contact pad at said 2nd contact pad, The step which deposits a catalyst nucleation layer on the front face of said 1st contact pad at least, The step which carries out growth formation of said two or more nano wires from said catalyst nucleation layer of said 1st contact pad at least, The approach containing the step which combines said nano wire which carried out growth formation with any of the nano wire by which growth formation was carried out on said 2nd contact pad or said 2nd contact pad they are, and offers said circuit apparatus which interconnected.
[Claim 6] The step which deposits said catalyst nucleation layer is an approach according to claim 5 characterized by including carrying out growth formation of said two or more nano wires from said catalyst nucleation layer on the front face of depositing said layer, said 1st contact pad, and the 2nd contact pad in said 1st contact pad and the 2nd contact pad.
[Claim 7] Said step which combines said nano wire, including further the step which impresses electric field and promotes growth formation of said nano wire in the direction in which erection aligned to said circuit base is an approach according to claim 6 characterized by including combining a nano wire between growth formation.
[Claim 8] Said step to combine is an approach according to claim 5 characterized by including van-der-Waals-attraction association between adjoining nano wires including said step which carries out growth formation of said nano wire carrying out growth formation of said nano wire for a long time than the one half of the magnitude of said clearance.

[Claim 9] The approach according to claim 8 characterized by including further the step which stimulates the physical contact between adjoining nano wires mechanically.
[Claim 10] The approach according to claim 8 of covering said nano wire with a conductive metal, and containing further the step which strengthens interconnect between said nano wires.
[Claim 11] At least, said 2nd contact pad is covered with the solder ingredient, and the step which carries out growth formation said nano wire It includes carrying out growth formation of said nano wire from said 1st contact pad. Said step which connects The approach according to claim 5 characterized by including heating said 2nd contact pad at least so that soldering association of said nano wire may be carried out at said 2nd contact pad.
[Claim 12] The approach according to claim 5 of impressing electric field and containing further the step which promotes growth of said nano wire towards erection having aligned to the front face of said 1st contact pad at least.
[Claim 13] Said step which aligns said two circuit bases is an approach according to claim 5 which forms the spacer which has predetermined height between said two circuit bases, and is characterized by including maintaining said two circuit bases by the relation as for which fixed spacing was vacant.
[Claim 14] Said catalyst nucleation layer is an approach according to claim 5 characterized by being conductivity.
[Claim 15] Said catalyst nucleation layer is an approach according to claim 5 characterized by manufacturing with the ingredient chosen from the group which consists of an alloy, carbide, a nitride, and a silicide.
[Claim 16] Said nano wire is an approach according to claim 5 characterized by including a heterojunction.
[Claim 17] Said step which carries out growth formation is an approach according to claim 5 characterized by carrying out before said step which aligns.
[Claim 18] It is the approach of manufacturing the circuit apparatus which interconnected, and is the step which offers at least two circuit bases. The step which at least one contact pad is prepared in each of said at least two circuit bases, and demarcates the 1st contact pad and the 2nd contact pad at least, The step which deposits a catalyst nucleation layer on the front face of said 1st contact pad and the 2nd contact pad, Said two circuit bases are aligned in the direction parallel to the real target which vacated spacing. Are the step which demarcates a clearance among them and in the step to which said 1st

contact pad meets and aligns at said 2nd contact pad, and the condition that electric field are impressed Growth formation of two or more nano wires is carried out from the front face of said 1st contact pad and the 2nd contact pad. Two or more nano wires by which are the steps which promote growth of said nano wire to the direction which intersected perpendicularly with said contact pad substantially, and growth formation is carried out from said 1st contact pad The approach containing the step which offers the circuit apparatus which combined with two or more nano wires by which growth formation is carried out from said 2nd contact pad, and interconnected by it.
[Claim 19] The approach according to claim 18 which aligns in the direction accumulated on said two or more nano wires by which at least three circuit bases were established and growth formation was carried out between the adjoining circuit bases, and is characterized by making a multilayer pile configuration.
[Claim 20] Interchange-circuit equipment manufactured by claim 1.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Both this inventions are transferred to the grantee of this application, and included in this specification by referring to. United-States-patent-apply [of the name "Tactile Sensor Comprising Nanowires and Method for Making the Same" for which the artificer Jin of this invention applied on September 24, 1999], and it reaches. The artificer Brown of this invention, and Jin and Zhu applied with this application. It relates to United States patent application of the name "Article Comprising Vertically Nano-Interconnected CircuitDevices and Method for Making the Same."
[0002] Especially this invention relates to a conductive nano wire, the structure which interconnected, and the approach of interconnecting in a original location about a minute interchange circuit and its manufacture approach.
[0003]
[Description of the Prior Art] For the diameter of 1-100 nanometers, nano-scale wires, such as a carbon nanotube with a die length of about 0.1-100 micrometers of a very small dimension, attract big attention,

and are in recent years. Liu et al., SCIENCE, Vol. 280, p. 1253 (1998); Ren et al., SCIENCE, Vol. 282, p. 1105 (1998); Li et al., SCIENCE, Vol. 274, p. 1701 (1996); Frank et al., SCIENTCE, Vol. 280, p. 1744 (1998); J. Tans etal., NATURE, Vol. 36, p. 474 (1997); Fan et al., SCIENCE, Vol. 283 and .512; (1999) Collins et al. and SCIENCE, Vol. 278 and p. 100; (1997) Kong et al., NATURE, and Vol. 395. P. 878; (1998) And Ebbesen et al., NATURE, Vol. 382, and p. 54 Reference (1996).

[0004] A carbon nanotube shows interesting physical characteristics, such as peculiar atomic arrangement, nano-scale structure and a single dimension-electrical-and-electric-equipment operation, quantum conductance, and ballistic transport properties. Frank etc. -- as reported, the ballistic transportation in a carbon nanotube is equal to the magnitude of the current density of some superconductors, or enables a lot of current passage in the electrical circuit in the magnitude of larger current density than it. A carbon nanotube is one of the nano wire ingredients of the lower limit which has a high aspect ratio generally. In the case of a single wall nanotube, in the case of -1nm and a multiwalled nanotube, these have a minor diameter below -50nm. Rinzler, etc. APPLIED PHYSICS, Vol. A67, and p. 29; (1998) Kiang, etc. J. PHYSICAL CHEM., Vol. 98, p. 6612 (1994) Kiang, etc. PHYSICALREVIEW LETTERS, Vol. 81, and p. 1869 Reference (1998).

[0005] Growth formation of the single wall carbon nanotube of high quality is usually carried out as a nanotube by laser ablation or the arc process by which orientation was carried out to arbitration and round which the shape of needlelike or noodles twined (in order to remove non-nanotube ingredients, such as the shape of a graphite, and an amorphous phase, a catalyst metal, etc., a chemical washing process is usually required for an arc generation carbon nanotube). Ren etc. -- Fan etc. -- and Li etc. -- chemical vapor deposition (CVD) which is used is in the inclination which generates the multiwalled nanotube in many cases accompanied by epitaxy formation of the half-alignment which stood straight to the substrate, or alignment attached in the substrate. When reaction parameters, such as temperature, time amount, precursor concentration, and a flow rate, are optimized as indicated by these reports, contact (catalyst) decomposition of hydrocarbon content precursors, such as ethylene, methane, or benzene, generates a carbon nanotube. Thin covering of nickel, Co, Fe, etc. A nucleation layer is the nanotube which a large number separated. In order to carry out nucleation, it is intentionally added to a substrate front face in many cases. A carbon nanotube is because the precursor of the hydrocarbon content mixed with the chemical entities (ferrocene etc.) containing one

or more of these catalyst metal atoms, for example is used, without using this metal nucleation layer, Nucleation can be carried out and growth formation can also be carried out. Between chemical vacuum deposition, these metal atoms play the role which carries out nucleation of the nanotube on a substrate front face. Cheng etc. -- CHEM. PHYSICS LETTERS, Vol. 289, and p. 602 reference (1998).

[0006]

[Problem(s) to be Solved by the Invention] The current trend in an electrical circuit design, interconnect, and packaging is going to use of a more detailed feature, and reached submicron feature size at recent years. In order to manufacture desired super-high density electronic packaging, circuit line breadth's being narrow and the three-dimensions multilayer configuration equipped with the vertical integration circuitry layer are important. However, the nano wire by which growth formation was carried out by the approach available now does not fit this purpose. With laser ablation or an arc process, single [that growth formation is carried out] wall nanotubes (SWNT), such as what was generally compounded, have the noodles-like configuration, and have twined mutually in many cases. In the parallel configuration which aligned, it is easy to manufacture the direction of multilayer nanotubes (MWNT), such as what is generally manufactured, with chemical vapor deposition. however, Ren etc. -- and Li etc. -- nanotubes [that these growth formation is carried out, such as what was reported,] differ in height or die length. In order to be reliable circuit interconnect without an electric short circuit and an electric circuit, it is equal and it is desirable to produce the nano wire which has specific predetermined die length. The application under coincidence connection of the name "Article Comprising Vertically Nano-Interconnected Circuit Devices and Method for Making the Same" for which the artificers Brown and Choi of this invention and Jin applied with this application equalizes the die length of a nano wire, and the manufacture technique which combines them with a circuit base for interconnect is indicated. However, probably, it will also be advantageous to provide the original location between circuit pads or between components with the approach of carrying out growth formation of the nano wire, and to avoid equalization and soldering by it.

[0007]

[Means for Solving the Problem] This invention contains at least two circuitry layers or circuit apparatus formed by any of an parallel configuration of having constituted or coexisted they are, and two or more nano interchange-circuit equipments which have been arranged among

them and which have the nano wire of equal die length substantially. Moreover, the manufacture approach including the original location growth formation of a nano wire by at least one of the circuit bases of an interworking unit of equipment is also indicated. The approach of original location growth formation offers the 1st and 2nd circuit bases at least, The thing which vacated spacing for these circuit bases and for which it aligns by parallel relation substantially and a clearance is demarcated among them, It includes carrying out growth formation of two or more nano wires from a catalyst nucleation layer so that depositing a catalyst nucleation layer on at least one of the circuit bases of these and two or more nano wires may be arranged between the 1st and 2nd bases. A nano [that growth formation is carried out] wire is combined so that interchange-circuit equipment may be formed. In 1 operation gestalt, a nano wire is combined by joining together, when carrying out growth formation and carrying out both growth formation from both 1st and 2nd bases. In another operation gestalt, a nano wire carries out growth formation from one side of a circuit base, and is soldered to the circuit base of another side. Furthermore, in another operation gestalt, when the 1st and 2nd circuit bases have aligned, a nano wire carries out growth formation so that an adjoining nano wire may interconnect overlap, next an adjoining nano wire by van-der-Waals-attraction association and the further electrical installation of arbitration. A perpendicular or level interconnect can be attained using this invention.

[0008]

[The gestalt of invention implementation] In order to make this invention easy to understand, an instantiation operation gestalt is explained below, referring to an attached drawing. The drawing referred to here aims at illustrating the concept of this invention, and please understand that it is not for limiting. The same sign used in a drawing means the same description.

[0009] The applicant discovered the approach of producing conductive nano wires, such as a carbon nanotube useful as a nano-scale which connects a wire between circuit apparatus layers. The approach explained in this specification includes the original location growth formation and interconnect of a nano wire on one or more circuit bases. Use of much small division parallel conduction pass can be attained using the nano wire which aligned for the interconnect between two circuitry layers or fitting equipment so that a circuit. In avoiding the problem of the short period and the long-term dependability which are caused by the stress which is not desirable, for example, a nano wire offers the

advantageous elastic compliance and the flexibility of an interconnect medium. The common generation source of the stress concerning an interconnect medium contains the mechanical stress and thermal stress which are generated during a local temperature gradient, the stress resulting from the mismatching of the coefficient of thermal expansion between different ingredients used for equipment, the stress by which induction was carried out to electromigration and equipment assembly, handling, a trial, or transportation. This invention avoids the problem of the dependability caused by fatigue of an interconnect medium or a circuit component, a creep, and this stress including deformation.

[0010] A nano wire is compoundable by various known approaches, such as chemical vacuum deposition of mixing of laser ablation, arc discharge, precursor gas, or precursor gas. It was transferred to the grantee of this application, respectively, and included in this specification by referring to here. It is United States patent application under connection in coincidence. By the artificer Jin of this invention Application of the name "Article Comprising Enhanced Nanotube Emitter Structure and Process for Fabricating Article" for which it applied on January 25, 1999, And application of the name "Tactile Sensor Comprising Nanowires andMethod for Making the Same" for which it applied on September 24, 1999, And the artificer Brown By Jin and Zhu, with this application Application of the name "Article Comprising Vertically Nano-Interconnected Circuit Devices and Method for Making the Same" for which it applied is referred to. These applications are indicating the method of manufacturing a nano wire, and the joint technique of performing perpendicular interconnect. when the approach indicated by this detail letter is used, growth formation is carried out and a nano wire interconnects in the original location on a circuit base. In this way, Brown under connection in the coincidence quoted above, and Jin and Zhu Equalization and a soldering joint process which were indicated in application are avoidable.

[0011] When a drawing is referred to, drawing 1 A - 1C is the schematic drawing showing the instantiation-process about original location growth formation of the nano wire between two circuit bases. drawing 1 -- A -- setting -- electric contact -- a pad -- 12 -- a -- 12 -- b -- 12 -- a -- ' -- and -- 12 -- b -- ' -- having -- two -- a ** -- fitting -- a circuit -- a base -- ten -- ten -- ' -- contact -- a pad -- mutual -- meeting -- as -- arranging -- having -- **** . The relative location of a corresponding contact pad (for example, 12a, 12a' and 12b, 12b') has aligned, and the base is held in the fixed position, in order to maintain spacing between alignment of a pad, and a desired pad. In

drawing 1 A - 1C, two circuitry layers meet mutually and are arranged. However, if it is a request, in order to attain multilayer pile configurations, such as high density and three-dimensions circuit structure, please understand that an additional layer may be accumulated, for example.

[0012] As for the catalyst nucleation layer 26, it is desirable to prepare alternatively on the front face of each contact pad so that growth formation of the nano wire may be alternatively carried out on a pad front face. A catalyst nucleation layer contains the thin film of the catalyst (contact) ingredient which usually has the thickness which has about 1-500nm in the range of 2-50nm still more suitably. A nucleation layer may be deposited by the known deposition approach in the enterprise fields concerned, such as sputtering, vacuum evaporationo, CVD, and electrochemical deposition. The instantiation catalyst ingredient which forms a nucleation layer contains the alloy of nickel, Co, Fe(s), or these ingredients. The catalyst ingredient should have conductivity, in order to use it in confirming circuit interconnect, for example, it may also contain a metal, an alloy, carbide, a nitride, or a silicide.

[0013] contact -- a pad -- 12 -- a -- 12 -- b -- 12 -- a -- ' -- 12 -- b -- ' -- manufacturing -- a thing -- using it -- an ingredient -- for example, -- aluminum -- Cu -- W -- Ta -- or -- CoSi -- two -- etc. -- a semiconductor circuit -- manufacture -- setting -- general -- using it -- an ingredient -- from -- it can choose . The selected pad ingredient should be stable at the processing temperature for CVD, and this temperature is usually in the range of 400-1000 degrees C. Although it can manufacture from carbide or a nitride as mentioned above in alternative, in this case, carbide or a nitride can play a role of metalization and a diffusion barrier, and, in a certain case, can play a role of a catalyst ingredient. Usually, after thin film deposition, a circuit base is in the condition by which patterning was carried out with the lithography technique in the contact pad on it, and is manufactured from semiconductor materials, such as Si, germanium, and GaAs. Area is under 25 square microns, as for the contact pads 12a and 12b etc., it is desirable that it is under a 1 square micron, and it is usually still more desirable that they are under 0.01 square microns. The configuration of a pad may be other configurations also with sufficient or reliance in a square, a rectangle, and a round shape rather than may be [for example,] important. Moreover, you may also include the matrix of the contact location which an parallel conductive strip is made to cross and is formed. In drawing 1 A, as for the

clearance between the requests between the fitting circuit base 10 and 10' "g", it is desirable that it is usually in the range of 0.01-500 microns, and is in the range of 0.1-100 microns, and it is still more desirable that it is in the range which is 0.2-10 microns. You may constitute from a binder course of the ceramic which could use the spacer 17 in order to maintain this clearance, could constitute this from film deposited on both a base 10, and 10both [one side or], or was placed among them, or a polymer.

[0014] A nano wire will be turned to the more nearly mutual one once the fitting base 10 and 10' align appropriately, as shown in drawing 1 A. Nucleation can be carried out and growth formation can be carried out. For example, drawing 1 B shows two nano wires 14 and 14 which are carrying out growth formation toward the more nearly mutual one. If a catalyst nucleation layer is deposited only on a contact pad, a nano wire will carry out growth formation only from the range of a pad, as illustrated, and will not carry out growth formation on the front face 18 between pads. As for a nano wire, it is advantageous to carry out growth formation on a pad front face at erection. As for the deviation from perfect perpendicular (erection) alignment, it is desirable that it is less than about 25 degrees from alignment with it, and it is still more desirable that it is less than about 15 degrees. [that desirable namely, it is small and] [perfect (90 degrees)] In order to promote the growth [****] which was parallel and aligned on a pad front face, external electric field may be applied. Although the field strength to apply is influenced by the ingredient of a nano wire, and the dimension (for example, a diameter, mechanical rigidity, and electrical characteristics) of the request, it is usually desirable that electric field are in the range of about 0.01-1000 volts/micron, and it is in the range of 1-200 volts/micron.

[0015] If CVD processing continues, the nano wire which carries out growth formation from the **** circuit base of a top or the bottom will contact. the bottom of existence of sufficient electric field -- a "basic growth mechanism" or a "chip growth mechanism" (S.Amelinckx etc. and SCIENCE Vol.265 (1994) --) As a pair of nano wire which approached showed the report by Fan and Li which were quoted by p.635 and the above to drawing 1 C according to related growth mechanisms, such as reference, they are the single nano wires 14a, 14b, and 14c... It may be combined to 14i. Original location perpendicular interconnect is carried out in this way, and is realized. All the nano wires or in order for all not to join together mostly and to confirm perpendicular interconnect, it is only required for a sufficient number of nano wires to join together.

[0016] The progressive approach about original location growth formation and interconnect of a nano wire is applicable also to the equipment property peculiar to nano wire processing shown in drawing 2 . The metal semi-conductor wire connected in the shape of a straight line may be used. For example, drawing 2 shows graphitized carbon nanotube 4a attached in the end of semi-conductor nano wire 4b. J. Hu etc. -- NATUREVol. 399 (1999) and p. 48 -- reference. A metal semi-conductor heterojunction can be made into one or more nano wires and one, and a role of adjustment diode equipment can be made to play. You may also build the equipment of other classes, such as p-n junction, transistor structure, or tunneling equipment structure, into a nano wire. By using momentary growth formation and a joint technique, the array of junction of a metal-semi-conductor-metal or semi-conductor-metal-semi-conductor can be attained. When growth formation of a nanotube is based on a chip growth mechanism, catalyst metal particles may be needed like [in under specific CVD composition conditions] with an advance nanotube chip. In this case, two nanotubes to combine may understand a catalyst particle in that internal cavity, or may emit them to a longitudinal direction, and growth formation and association may be continued, or a catalyst particle may contact, and association (CVD temperature high enough van-der-Waals-attraction association or diffusion association) of a metal pair metal may be formed. A semiconductor region or a heterojunction can be guided for whether a catalyst particle is understood or when emitted partially, this very thing can apply stress locally by blocking the atomic arrangement of a nano wire in such a location, and the bent field.
[0017] Drawing 3 A and 3B show the alternative instantiation-process about original location growth formation and perpendicular interconnect. Here, a spacer 17 can be used, in order that two circuit bases 10 and 10' may prepare as mentioned above, may align and may maintain this alignment. nano -- a wire -- one side -- a circuit -- a base -- ten -- contact -- a pad -- 12 -- a -- 12 -- b -- a top -- growth -- formation -- carrying out -- a catalyst -- nucleation -- a layer -- 26 -- covering -- on the other hand -- another side -- a circuit -- a base -- ten -- ' -- contact -- a pad -- 12 -- a -- ' -- 12 -- b -- ' -- the solder ingredient 38 -- covering . A solder ingredient can be used as Au-Sn, Sn-Ag, Sn-Sb, Pb-Sn, Bi-Sn, In-Sn, In-Ag eutectic solder, or other solder that are known for the technical field concerned. When high temperature processing like CVD which comes out -500, for example is required for composition of a nano wire, the solder layer ingredient should be chosen from high-melting alloys, such as brazing solder or a soldering alloy well known for the technical field concerned. In the

case of a carbon nanotube, or nitride type a nano wire / nanotube, a solder ingredient may be used as the alloy of one or more little carbide formation elements, such as Ti, Mo, Cr, Nb, V, Fe, W, Zr, and Ta, or a nitridation element in order to improve the wetting of a nano wire with the solder ingredient 38. Here, a nano wire is from one side of two bases 10. Carrying out nucleation, growth formation is carried out (drawing 3 A), and, finally a nano wire gains sufficient die length to contact the solder ingredient 38 (drawing 3 B). Once contact is performed (for example, drawing 3 B), the structure can be heated, soldering association of the nano wire chip can be carried out at the solder layer 38, and perpendicular-unification can be completed.

[0018] Drawing 4 A - 4C shows the alternative instantiation-process about the original location growth formation and perpendicular interconnect which are performed by removing the impressed electric field, before the nanotube which carries out growth formation mutually and approaches from the direction which counters approaches mutually. When there are no electric field, possibility that the circuit base 10 which counters, and the nano wire which approaches from 10' will join together is far low, and, for this reason, the structure of drawing 4 A is attained by the nano wire which passes mutually, for example. Since the van-der-Waals-attraction association 15 may occur as shown in drawing 4 B, with the nano wire of a single wall, or the thin nano wire of other walls, a nano wire contacts mutually especially by stimulating the physical contact between the nano wires which adjoin automatically. Physical contact may stimulate applying airstream or a nano wire through other techniques vibrated mechanically. Parallel installation of the nano wire by van-der-Waals-attraction association is advantageous about especially dependability when such large stress that it is not desirable and the hauling force which may be caused by the mismatching of a big thermal expansion of dissimilarity circuit ingredient or base ingredient are applied accidentally. Although the attached wire receives mutually, it can only be slid on it and electric contact is maintained under this situation, the big hauling force is adjusted without damaging a nano wire. although it appears in the van-der-Waals-attraction association itself attaining desired perpendicular interconnect enough, if the further electric interconnect and lower resistance are desired -- the stress modulation ability of the parallel installation configuration of drawing 4 B -- a little -- or -- adhesion of a nano wire may be strengthened further, making it a sacrifice. for example, the conductive metal 16 is for example, CVD metal deposition or electrochemical deposition, and was shown in drawing 4 C -- as -- at least -- some wires

-- it deposits upwards.
[0019] In alternative, first, after a nano wire carries out growth formation according to an individual on two **** circuit bases 10 and 10', it may align a circuit, it may be arranged so that it may meet mutually, and as shown in drawing 5 A, each other may be brought close. As for a nano wire, it is desirable to carry out growth formation mostly in the form which aligned in parallel by erection, and when the die length of the nano wire on each base doubles a base like for example, drawing 5 A, a ******** is more desirable than the one half of a clearance (g) so that the die length which the nano wire combined may become longer than a clearance (drawing 5 B). Thus, especially, when the diameter of a nano wire is small (for example, less than 10nm), as shown in drawing 5 B, it generates between the nano wires with which the van-der-Waals-attraction association 15 adjoins, and perpendicular electric interconnect is enabled. Moreover, when it desires the further electric interconnect and lower resistance, a nano wire may be further combined, as explained above with reference to drawing 4 C. The die length of the nano wire on each base is under one half of a clearance (g), therefore when each base 10 and the nano wire on 10' did not contact, as these nano wires showed drawing 4 A, CVD can be used in the condition that electric field are impressed so that growth formation may be carried out, it may join together and it may become each nano wire, and growth formation of these nano wires can be carried out further.
[0020] Original location growth formation and the interconnect technique of this invention are applicable also to confirming level circuit interconnect. The instantiation-approach of performing this interconnect was shown in drawing 6 A - 6C. First, in drawing 6 A, the base 100 which consists of other ingredients known in the technical field which manufactures Si, SiO2, SiN4, or a semiconductor wafer, for example and which may contain a semiconductor wafer is established. This base may also contain various circuit components, such as equipments, such as the source, a drain, the gate or diode, and a transistor. A base or a circuit may be covered with metalization layers, such as a layer of Cu, aluminum, W, Ta, or CoSi2. As shown in drawing 6 A, as long as it is required, the ingredient of Fe, Co and nickel which were mentioned above, for example about this layer, carbide, or a nitride may be used, and patterning of the catalyst nucleation layer 26 may be applied and carried out. As for a catalyst nucleation layer, it is advantageous to manufacture like [in the case of using TiN or a TaN layer] with the ingredient which can also play a role of a diffusion barrier for semiconductor circuits. Next, patterning of a metalization layer and the

catalyst nucleation layer is carried out with a lithography technique, and they are made a desired circuit line and a desired pad configuration, and in order to offer the structure shown in drawing 6 A, they are covered with the dielectric (insulation) layers 102, such as SiO2 or SiN4.

[0021] As shown in drawing 6 B next, a laser beam or lithography processing is used and the level slot 104 is deeply cut to the layer structure of drawing 6 A. In this way, the cross section of a catalyst nucleation layer is exposed. A nano wire is this exposed front face. Carrying out nucleation and carrying out growth formation horizontally may be permitted. As shown in drawing 6 B, electric-field $\tilde{E}$ may be impressed over the whole slot so that growth formation may be carried out and it may join together in the form where the nano wire 14 aligned. Thus, equipment functions, such as p-n junction, a tunnel junction, and a rectifier, can be introduced into a slot area according to specific design needs. The direction of electric field may be corrected so that a slot which promoted growth of a nano wire in the different direction, and is different in alternative may be interconnected. In order to add interconnect or to create the interconnect to other slots, CVD processing of the circuit assembly may be carried out further. As shown in drawing 6 C, an additional circuit or additional equipments 40 (for example, multilayer damask inlaid work structure etc.) may be combined with final structure by the flip chip soldering association 42.

[0022] The operation gestalt explained on these specifications is only known [instantiation] by that much deformation and corrections can be made, without this contractor deviating from the main point and range of this invention. The applicant has the intention of these deformation and corrections being included in an attached claim. [all]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1 A] It is the schematic drawing showing the instantiation-process about original location growth formation of the nano wire between two circuit bases.

[Drawing 1 B] It is the schematic drawing showing the instantiation-process about original location growth formation of the nano wire between two circuit bases.

[Drawing 1 C] It is the schematic drawing showing the instantiation-process about original location growth formation of the nano wire between two circuit bases.
[Drawing 2] It is the schematic drawing showing the original location perpendicular interworking unit which has the nano wire equipped with the heterojunction.
[Drawing 3 A] It is the schematic drawing showing the alternative instantiation-process about original location growth formation of the nano wire between two circuit bases.
[Drawing 3 B] It is the schematic drawing showing the alternative instantiation-process about original location growth formation of the nano wire between two circuit bases.
[Drawing 4 A] It is the schematic drawing showing the alternative instantiation-process about original location growth formation of the nano wire between circuit bases.
[Drawing 4 B] It is the schematic drawing showing the alternative instantiation-process about original location growth formation of the nano wire between circuit bases.
[Drawing 4 C] It is the schematic drawing showing the alternative instantiation-process about original location growth formation of the nano wire between circuit bases.
[Drawing 5 A] It is the schematic drawing including growth formation of a fitting circuit base-like nano wire, and connecting a fitting base showing an instantiation-process.
[Drawing 5 B] It is the schematic drawing including growth formation of a fitting circuit base-like nano wire, and connecting a fitting base showing an instantiation-process.
[Drawing 6 A] It is the schematic drawing showing the instantiation-process about the original location growth formation of a nano wire for manufacturing level interchange-circuit equipment.
[Drawing 6 B] It is the schematic drawing showing the instantiation-process about the original location growth formation of a nano wire for manufacturing level interchange-circuit equipment.
[Drawing 6 C] It is the schematic drawing showing the instantiation-process about the original location growth formation of a nano wire for manufacturing level interchange-circuit equipment.
[Description of Notations]
4a Graphitized carbon nanotube
4b Semi-conductor nano wire
10 10' Fitting circuit base
12a, 12a', 12b, 12b' Electric contact pad

14, 14a, 14b, 14c, 14d, 14e, 14f, 14g, 14h, 14i Nano wire
15 Van-Der-Waals-Attraction Association
16 Conductive Metal
17 Spacer
18 Front Face
26 Catalyst Nucleation Layer
38 Solder Ingredient
40 Additional Circuit or Equipment
42 Flip Chip Soldering Association
100 Base
102 Dielectric (Insulation) Layer
104 Level Slot